IN THE CLAIMS

1. (Original) A method of context switching between processes in a computer operating system including writing cached data back to a memory means, comprising the step of the writing cached data back to the memory means during processor idle cycles at completion of a process and prior to initiation of the context switch.

2. (Original) A method as claimed in Claim 1, including the step of setting a flag to indicate cached data has been written back to memory subsequent to the completion of the process.

3. (Original) A method as claimed in Claim 2, including the step of, at the time of requiring a context switch, checking for the said flag to identify if the previous process's cached data has been written back to memory.

4. (Original) A method as claimed in Claim 3, including the step of, upon identifying that the said flag has been set, conducting the context switch without further cache write-back to memory.

5. (Original) A method as claimed in Claim 3, and including the step of conducting a cached data write-back to memory at the time of requiring a context switch if the said flag has not been identified as set.

6. (Original) A computer implemented system including a processor and cache memory arranged to receive operating system instructions for context switching between processes, and including control means for writing back cache data to memory means during processor idle cycle at completion of a process, and prior to initiation of the context switch.

7. (Original) A system as claimed in Claim 6, and arranged to employ a processor sleep mode to write cache data back to memory automatically during a sleep period.

8. (Original) A system as claimed in Claim 6, and including a status register having a flag for initiating data cache write-back during a CPU sleep operation.

9. (Original) A system as claimed in Claim 6, wherein the operating system is arranged with an additional sleep code instruction for the data cache write-back

10. (Original) A system as claimed in Claim 9, wherein the sleep code of the processor includes an additional data cache write-back instruction.

11. (Original) A computer program product having computer program instructions and arranged for controlling context switching between processors in a computer operating system so as to write cached data back to memory means during processor idle cycles at completion of a process and prior to initiation of the context switch.

12. (Cancel)